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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/808,710	03/14/2001	Michael B. Jacobson	10971442-1	5820

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2133	3

DATE MAILED: 12/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/808,710	JACOBSON, MICHAEL B.	
	Examiner	Art Unit	
	James C Kerveros	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1, with respect to claimed limitation "when performing a particular parity operation, determining which of the stored subsets of parity coefficients is needed for the particular parity operation", the phrase "when performing a particular parity operation" renders the claim indefinite because the term "when" fails to define the particular time in relation to the parity operation, since it is unclear whether the limitation following the phrase is part of the claimed invention. An Examiner's proposed corrected claim is as follows: "determining which of the stored subsets of parity coefficients is needed for a particular parity operation".

However, for examination purpose, the Examiner applies the proposed corrected claim.

Also, claims 5-6 are rejected because they depend from a rejected main claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 6-8, 10, 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Chiang (US 6594796).

Regarding independent Claims 1, 10, Chiang discloses a method and system for processing ECC P-and Q-parity check bytes for a memory array (11, Figure 1), in a redundant data storage system that utilizes a plurality of data segments, and at least two corresponding parity segments, such as two ECC P- and Q- parity check bytes, where each data element is read by an ECC-P and -Q processors, comprising:

Pre-selecting parity coefficient subsets by determining P-parity coefficients s0[n1] and s1[n1] and Q-parity coefficients s0'[n1] and s1'[n1], as shown in Figures 5-8, for stream of data element values s(k) (k=0, 1, . . . , R-1) from a memory array (11, Figure 1) for use in different parity operations, such as parity error generation, see Figures 13 and 14.

Storing all of the pre-selected parity coefficient subsets in memory (135, 137, Figure 13) for the P-parity coefficients and in memory (145, 147, Figure 14) for the Q parity coefficients, respectively, after they have undergone weighted summation.

Determining and reading the subset of parity coefficients (P- s0 and Q- s0') from the memory, to determine which of the stored subsets (P and Q) of parity coefficients

(s0 and s0') are required for a particular parity operation. The components s0 [n1] and s1 [n1] are read out and received by the processing module 130, shown in Figure 13, to compute the P-parity code words c0 [n1] and c1 [n1], as indicated in the relations (6) and (7). Similarly, the components s0' [n2] and s1' [n2] are read out and received by processing module 140, analogous to 130 in Figure 13, and the corresponding components 141, 143, 145 and 147, in Figure 14 to form the Q-parity code words c0' [n2] and c1' [n2], which are computed according to the relations (31) and (32). And, also, performing the particular parity operation with the subset of parity coefficients (s0 and s0') that was read from the memory.

Regarding Claim 2, 11, Chiang discloses a storing step comprising, using pre-formatted data from memory array (11, Figure 1) for storing the parity coefficients to memory array (135, 137) for P-parity and memory array (145, 147) for Q-Parity error. The parity operation is accomplished by hardware-based parity operation logic, such as ECC-P an ECC-Q processor for forming the ECC-P-parity and ECC-Q-parity check bytes, using shift registers with feed-back and/or weighted summation of selected register contents, that utilizes the subsets of parity coefficients as they are pre-formatted in the memory array.

Regarding Claims 6-8, Chiang discloses the common limitation recited in the independent claim 1, above, and in he discloses the step of calculating an offset, such as an index "k", by receiving the data element value s(k) (k=0, 1, . . . , R-1) at the input of MUX 51, corresponding to P-parity coefficients s0[n1], which is provided with the index "k" and feeding the data element value s(k) to the sum module SUM1-p (p=0, 1, . . . , N-1), which forms a sum of this received value, Figure 5-6. Also, the P-parity coefficients

s1[n1] element values s(k) (k=0, 1, . . . , R-1) are received at the multiplexer 61 and selectively feeding the data value s(k) and the index value k to one of the sum modules. The same data index is applicable to Q-parity coefficients for s0'[n2] and s1'[n2], Figures 7-8. Then, Chiang discloses the step of storing the calculated values with the index in the linear memory array (135, 137) for P-parity and linear memory array (145, 147) for Q-Parity error, corresponding to a subset size and then reading the subset values from the particular group corresponding to the calculated offset in the linear memory array

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 4, 5, 12, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang (US 6594796) in view of Davis (US 5819109).

Regarding Claims 3, 4, 5, 12, 13, Chiang substantially discloses classifying the different parity operations into classifications, including:

Parity segment generation, such as generating Error Correction Control (ECC) P- and Q-parity check bytes, for the data segments in memory array (11, Figure 1).

Parity segment regeneration, such as shown in Figures 9-12, illustrating an apparatus for processing the data elements s(k) (k=0000, 0001, . . . , R-1) to determine P-

parity and Q-parity check bytes, where a new sum is formed based on new data element value.

Wherein each classification includes a plurality of different classification scenarios involving a respective set of parity coefficients (P- s0 and Q- s0'), pre-selecting parity coefficient subsets (P- s0 and Q- s0') and for each of the different classification scenarios using pre-formatted data from memory array (11, Figure 1) for storing the parity coefficients to memory array (135, 137) for P-parity and memory array (145, 147) for Q-Parity error. The parity operation is accomplished by hardware-based parity operation logic, such as ECC-P an ECC-Q processor for forming the ECC-P-parity and ECC-Q-parity check bytes, using shift registers with feed-back and/or weighted summation of selected register contents, that utilizes the subsets of parity coefficients as they are pre-formatted in the memory array.

Regarding Claims 3, 4, 5, 12, 13, Chiang does not explicitly disclose "d*ata segment reconstruction operations*" . However, in analogous art, Davis (US 5819109) discloses a method of writing data to a storage system using a redundant array of independent/inexpensive disks ("RAID") comprising a reconstruction step, of a system failure occurring during a data write or after the data write, then the original data can be accurately reconstructed using the remaining data blocks and the original parity information that remains in the parity block.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the d*ata segment reconstruction method*, as taught by Davis, in the method of Chiang, for performing data *segment* reconstruction operations, since Davis eliminates the write hole problem of regenerating undetected corrupt data, and

additionally, it overcomes the need for system overhead to synchronize data writes to LBNs that map to the same parity block.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James C Kerveros whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4900.

James C Kerveros
Examiner
Art Unit 2133

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By: 12/10/03

Date: 10 December 2003
File: Non-Final Rejection

Guy J. Lamarre
for
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Primary Examiner